What is claimed is:

1. A nonvolatile semiconductor memory comprising:

a main memory cell array;

a sub-memory cell array; and

an address memory,

wherein, in case of a rewrite operation rewriting a portion of data written in the main memory cell array, a modification data is written into the sub-memory cell array without erasing said main memory cell array, and correspondent information on a first address of the main memory cell array storing a data to be modified and a second address of the sub-memory cell array storing the modification data is recorded in the address memory.

2. The nonvolatile semiconductor memory according to claim 1, further comprising:

an address management circuit which, at the time of a readout operation, compares a readout address with the first address of the correspondent information, and outputs the readout address when the comparison result indicates inconsistency, and outputs the second address of said correspondent information when the comparison result indicates consistency.

3. The nonvolatile semiconductor memory according to claim 1, further comprising:

a rewrite mode decision circuit which detects a rewrite

operation mode in response to an external signal,

wherein, on detection of the rewrite operation mode, the modification data is written into the sub-memory cell array, and the correspondent information is recorded into the address memory.

4. The nonvolatile semiconductor memory according to claim 1,

wherein, in response to a supplied write data and a supplied write address, a data in the main memory cell array corresponding to the write address is compared with the write data, and when the write data can be written into the main memory cell array, the supplied write data is written into said main memory cell array, and when the write data cannot be written into the main memory cell array, the supplied write data is written into the sub-memory cell array, and also the correspondent information is recorded into the address memory.

5. The nonvolatile semiconductor memory according to claim 1, further comprising:

a memory block having the main memory cell array and the sub-memory cell array,

wherein, at the time of an erase operation, data stored in both the main memory cell array and the sub-memory cell array within the memory block are erased together.

6. The nonvolatile semiconductor memory according to claim 5, further comprising:

a plurality of the memory blocks,

wherein, at the time of the erase operation, the data stored within a selected memory block are simultaneously erased.

7. The nonvolatile semiconductor memory according to claim 1,

wherein, in the erase operation, the data stored in memory cells of the main memory cell array are simultaneously erased.

8. The nonvolatile semiconductor memory according to claim 1, further comprising:

an effective data memory storing an effective flag indicating which of the data before rewriting or the data after rewriting is effective,

wherein, at the time of a readout operation, when a first flag indicating the data before rewriting is effective is stored in the effective data memory, a data corresponding to the supplied readout address is read out from the main memory cell array, and

when a second flag indicating the data after rewriting is effective is stored in the effective data memory, if the readout address is consistent with the first address included in the correspondent information, a data of the

second address corresponding to the readout address is read out from the sub-memory cell array, or if the readout address is inconsistent with the first address, a data of the readout address is read out from the main memory cell array.

9. A nonvolatile semiconductor memory comprising:

a main memory cell array in which entire memory cells are set into an erase state by an erase operation, and a first data is written when the memory cells lie in the erase state;

a sub-memory cell array in which, at the time of a rewrite operation modifying a portion of the first data written in the main memory cell array into a second data, said modifying second data is written; and

an address memory which stores correspondent information on a first address of the main memory cell array storing a data to be modified and a second address of the sub-memory cell array storing the second data, when said second data is written into the sub-memory cell array.

10. The nonvolatile semiconductor memory according to claim 9,

wherein, at the time of a readout operation, a readout address is compared with the first address of the correspondent information, and when the comparison result indicates inconsistency, the first data corresponding to the readout address is output, and when said comparison

result indicates consistency, the second data corresponding to the second address of said correspondent information is output.

11. The nonvolatile semiconductor memory according to claim 9, further comprising:

a rewrite mode decision circuit which detects a rewrite operation mode in response to an external signal,

wherein, on detection of the rewrite operation mode, the second data is written into the sub-memory cell array and the correspondent information is recorded into the address memory.

12. The nonvolatile semiconductor memory according to claim 9,

wherein, in response to a supplied write data and a supplied write address, a data stored in the main memory cell array corresponding to the write address is compared with the write data, and when the second data can be written into the main memory cell array, the supplied second data is written into said main memory cell array, and when the second data cannot be written into the main memory cell array, the supplied second data is written into the sub-memory cell array, and also the correspondent information is recorded into the address memory.

13. The nonvolatile semiconductor memory according

to claim 9, further comprising:

a memory block having the main memory cell array and the sub-memory cell array,

wherein, at the time of an erase operation, data stored in both the main memory cell array and the sub-memory cell array in the memory block are erased together.

14. The nonvolatile semiconductor memory according to claim 9, further comprising:

an effective data memory storing an effective flag indicating which data of the first data or the second data is effective,

wherein, at the time of a readout operation, when a first flag indicating the first data is effective is stored in the effective data memory, the first data corresponding to the supplied readout address is read out from the main memory cell array, and

when a second flag indicating the second data is effective is stored in the effective data memory, if the readout address is consistent with the first address of the correspondent information, the second data of the second address corresponding to the readout address is read out from the sub-memory cell array, or if the readout address is inconsistent with the first address, the first data of the readout address is read out from the main memory cell array.